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These needs are met by the invention, which simultaneously generates and concatenates or interleaves two 8-bit PRNs within a single clock cycle. A first 8-bit PRN component is generated by a first eight-bit PRN device on a rising clock signal; a second 8-bit PRN component is generated on a falling clock signal of the same cycle by a second, independent eight-bit PRN device; and the two 8-bit PRN components are concatenated or interleaved to provide a 16-bit PRN that is issued for that clock cycle. The characteristic polynomials used for the first and second eight-bit PRN devices are preferably the same but may be independently chosen, as long as at least one polynomial is irreducible.

### Brief Description of the Drawings

Figures 1A and 1B schematically illustrate conventional generation of an 8-bit PRN.

Figures 2 and 3 schematically illustrate generation of 16-bit PRNs according to two embodiments of the invention.

### Description of Best Modes of the Invention

Figure 1 schematically illustrates a conventional system 11 for generating an 8-bit PRN within one clock cycle, using type D flipflops that are triggered on a rising clock signal edge. The particular LFSR configuration shown in Figure 1 corresponds to the characteristic polynomial

$$p_1(x;8) = 1 + x^2 + x^3 + x^4 + x^8, \quad (1)$$

where  $x$  is an unspecified element of a field and a "1" coefficient (always present) for the highest degree ( $x^8$ ) indicates that this stage is connected to a stage in another level. The system 11 shown in Figure 1, corresponding to the characteristic polynomial  $p(x;8)$  in Eq. (1), has 255 different non-zero value  $n$ -tuples ( $v_0, v_1, v_2, v_3, v_4, v_5, v_6, v_7$ ) (with  $n = 8$ ) and has a minimum cycle length of 255. The cycle generated by this LFSR system is irreducible in the sense that the polynomial  $p_1(x;8)$  cannot be expressed as the product of two or more polynomials of degree less than 8. S.B. Wicker, in Error Control Systems for Digital Communication and Storage, Prentice Hall, Upper Saddle River, NJ, 1995, pp. 445-447, lists 16 degree-8 irreducible polynomials:

$$p(x;8) = 1 + x^4 + x^5 + x^6 + x^8;$$

$$p(x;8) = 1 + x^3 + x^5 + x^7 + x^8;$$

$$p(x;8) = 1 + x^3 + x^5 + x^6 + x^8;$$

$$p(x;8) = 1 + x^2 + x^5 + x^6 + x^8;$$

$$p(x;8) = 1 + x^2 + x^4 + x^5 + x^6 + x^7 + x^8;$$

$$p(x;8) = 1 + x^2 + x^3 + x^7 + x^8;$$

$$p(x;8) = 1 + x^2 + x^3 + x^6 + x^8;$$

$$p(x;8) = 1 + x^2 + x^3 + x^5 + x^8;$$

$$p(x;8) = 1 + x^2 + x^3 + x^4 + x^8;$$

$$p(x;8) = 1 + x^2 + x^6 + x^7 + x^8;$$

$$p(x;8) = 1 + x + x^5 + x^6 + x^8;$$

$$p(x;8) = 1 + x + x^3 + x^5 + x^8;$$

$$p(x;8) = 1 + x + x^2 + x^7 + x^8;$$

$$p(x;8) = 1 + x + x^2 + x^5 + x^6 + x^7 + x^8;$$

$$p(x;8) = 1 + x + x^2 + x^3 + x^6 + x^7 + x^8; \text{ and}$$

$$p(x;8) = 1 + x + x^2 + x^3 + x^4 + x^6 + x^8. \quad (2)$$

In Figure 1, a reset signal is received or a feedback digital signal S(in) is received on an input signal line 13 and distributed to a data signal input terminal of each of eight type D flipflops (FFs), numbered 17-i (i = 0, 1, ..., 7). A clock signal CLK(t) is received on a clock input signal line 15 and is distributed to a clock input terminal each of the eight FFs 17-i. A single bit first output signal S(t;i;out1) (i = 0, 1, 2) from the FF 17-i is received by one of three input terminals of an AND gate 21 that forms and issues a first intermediate output signal S(t;0/1/2;out1) = S(t;0;out1)·S(t;1;out1)·S(t;2;out1). A single bit output signal S(t;i;out) (i = 3, 4, 5, 6) from the FF 17-i is received by one of three input terminals of an AND gate 23 that forms and issues a second intermediate output signal S(t;3/4/5/6;out1) = S(t;3;out1)·S(t;4;out1)·S(t;5;out1)·S(t;6;out1). These first and second intermediate output signals are received by a two-terminal OR gate 25 that forms and issues a third intermediate output signal

$S(t;0/1/2/3/4/5/6;out1) = S(t;0/1/2;out1) \oplus S(t;3/4/5/6;out1)$ . An output of the OR gate 25 is received by a first input terminal of an XOR gate 27.

A complementary single-bit output signal  $S(t;j1;out2) = S(t;j2;out1)^*$  is issued by the FFs 17-j1 ( $j1 = 1,2,3$ ) and is received by a first input terminal of an XOR gate 19-(j1+1).

A complementary single-bit second output signal  $S(t;j2;out2) = S(t;j2;out1)^*$  ( $j2 = 0, 4, 5, 6$ ) is issued by the FF 17-j2 and is received by a signal input terminal of the FF 17-(j2+1). A single bit complementary output signal  $S(t;7;out2) = S(t;7;out1)^*$  is issued by the FF 17-7 and is received by a second input terminal of the XOR gate 27. The output signal of the XOR gate 27 is fed back to, and received by, a second input terminal of the XOR gates 19-2, 19-3 and 19-4 and by the signal input terminal of the FF 17-0. The output signals  $S(t;j3;out2)$  ( $j3 = 0, 1, 2, 3, 4, 5, 6, 7$ ), collectively referred to as  $S(t;out)$ , are received in serial order by an output signal line 29 as an eight-bit pseudo-random number (PRN) from the device 11. The configuration shown in Figure 1 provides an eight-bit PRN  $S(t;out)$  with each clock cycle. Using any of Eqs. (2) for the characteristic polynomial, the system 11 generates an ordered sequence of 255 different, non-zero value n-tuples ( $n = 8$ ).

Figure 2 schematically illustrates a system 111 for generating a 16-bit PRN  $S(t;out)$  within one clock cycle according to the invention, using a first 8-bit LFSR 112A that is triggered on a rising clock signal edge and a second 8-bit LFSR 112B that is triggered on a falling clock signal edge during the same clock cycle. The particular LFSR configurations shown in Figure 2 correspond to the (same) irreducible characteristic polynomial, for example,

$$pA(x;8) = pB(x;8) = 1 + x^2 + x^3 + x^4 + x^8. \quad (3)$$

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10		15	
Year	Value	Year	Value
1990	10.0	1990	15.0
1991	10.5	1991	15.5
1992	11.0	1992	16.0
1993	11.5	1993	16.5
1994	12.0	1994	17.0
1995	12.5	1995	17.5
1996	13.0	1996	18.0
1997	13.5	1997	18.5
1998	14.0	1998	19.0
1999	14.5	1999	19.5
2000	15.0	2000	20.0
2001	15.5	2001	20.5
2002	16.0	2002	21.0
2003	16.5	2003	21.5
2004	17.0	2004	22.0
2005	17.5	2005	22.5
2006	18.0	2006	23.0
2007	18.5	2007	23.5
2008	19.0	2008	24.0
2009	19.5	2009	24.5
2010	20.0	2010	25.0
2011	20.5	2011	25.5
2012	21.0	2012	26.0
2013	21.5	2013	26.5
2014	22.0	2014	27.0
2015	22.5	2015	27.5
2016	23.0	2016	28.0
2017	23.5	2017	28.5
2018	24.0	2018	29.0
2019	24.5	2019	29.5
2020	25.0	2020	30.0
2021	25.5	2021	30.5
2022	26.0	2022	31.0
2023	26.5	2023	31.5
2024	27.0	2024	32.0
2025	27.5	2025	32.5
2026	28.0	2026	33.0
2027	28.5	2027	33.5
2028	29.0	2028	34.0
2029	29.5	2029	34.5
2030	30.0	2030	35.0
2031	30.5	2031	35.5
2032	31.0	2032	36.0
2033	31.5	2033	36.5
2034	32.0	2034	37.0
2035	32.5	2035	37.5
2036	33.0	2036	38.0
2037	33.5	2037	38.5
2038	34.0	2038	39.0
2039	34.5	2039	39.5
2040	35.0	2040	40.0
2041	35.5	2041	40.5
2042	36.0	2042	41.0
2043	36.5	2043	41.5
2044	37.0	2044	42.0
2045	37.5	2045	42.5
2046	38.0	2046	43.0
2047	38.5	2047	43.5
2048	39.0	2048	44.0
2049	39.5	2049	44.5
2050	40.0	2050	45.0
2051	40.5	2051	45.5
2052	41.0	2052	46.0
2053	41.5	2053	46.5
2054	42.0	2054	47.0
2055	42.5	2055	47.5
2056	43.0	2056	48.0
2057	43.5	2057	48.5
2058	44.0	2058	49.0
2059	44.5	2059	49.5
2060	45.0	2060	50.0
2061	45.5	2061	50.5
2062	46.0	2062	51.0
2063	46.5	2063	51.5
2064	47.0	2064	52.0
2065	47.5	2065	52.5
2066	48.0	2066	53.0
2067	48.5	2067	53.5
2068	49.0	2068	54.0
2069	49.5	2069	54.5
2070	50.0	2070	55.0
2071	50.5	2071	55.5
2072	51.0	2072	56.0
2073	51.5	2073	56.5
2074	52.0	2074	57.0
2075	52.5		

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received at the input terminal of the FF 157-(i4+1) and by the output line 131. A Q\* output signal from the FF 117-7 is received by a second input terminal of the XOR 127 and by the output line 131.

An output signal on an intermediate line 129 from the XOR gate 127 is fed to an input signal terminal of the FF 157-0 (analogous to feedback to the first FF 17-0 in Figure 1). This fed-back signal on the line 129 is also received and processed by a second input terminal of the XOR gates 159-i5 (i5 = 2, 3, 4); and the output signal of the XOR gate 159-i5 is received by a data input terminal of the FF 157-i5.

A Q output signal from the FF 157-i6 (i6 = 0, 4, 5, 6) is received by the FF 117-(i6+1) and by the output line 131. A Q output signal from the FF 157-i7 (i7 = 1, 2, 3) is received by the XOR gate 119-(i7+1) and by the output line 131. A Q\* output signal from the FF 157-i8 (i8 = 0, 1, 2) is received by a three-input terminal AND gate 161. A Q\* output signal from the FF 157-i9 (i9 = 3, 4, 5, 6) is received by a four-input terminal AND gate 163. The output signals from the AND gates 161 and 163 are received by two input terminals of an OR gate 165, whose output signal is received by a first input terminal of an XOR gate 167. The output line 131 and a second input terminal of the XOR gate 167 receive a Q output signal from the FF 157-7. An output signal from the XOR gate 167 is received on a signal line 169 by a control or clock signal terminal of the FF 117-0.

Eight bits of a 16-bit output signal S(t;out) are provided by one output signal (Q\*) from each of the FFs 117-i (i = 0, 1, ... , 7), and these bits are issued on a rising clock signal (or on a falling clock signal). Another eight bits of the 16-bit output signal S(t;out) are provided by one output signal (Q) from each of the FFs 157-i (i = 0, 1, ... , 7), and these bits are issued on a falling clock signal (or on

a rising clock signal). Optionally, the output signals from the FFs 117-i and/or the output signals from the FFs 157-i ( $i = 0, 1, \dots, 7$ ) are passed through delay modules with selected time delays to control any race problem that might otherwise occur. The entire 16 bits of the output signal  $S(t;out)$  are thus issued within a single clock cycle, after computation within a preceding clock cycle. The eight bits ( $Q^*$ ) issuing from the FFs 117-i and the eight bits ( $Q$ ) issuing from the FF 157-i may be interleaved in an arbitrary manner or may be concatenated to provide a 16-bit PRN that does not repeat itself for any cycle of length at least 255 and no greater than 65,535.

The two n-tuples provided by the LFSR configurations 112A and 112B can be concatenated to provide the following concatenated sequences, among others:

$$C1 = (v0, v1, v2, v3, v4, v5, v6, v7, v8, v9, v10, v11, v12, v13, v14, v15), \quad (4)$$

$$C2 = (v8, v9, v10, v11, v12, v13, v14, v15, v0, v1, v2, v3, v4, v5, v6, v7). \quad (5)$$

The two n-tuples provided by the LFSR configurations 112A and 112B can be interleaved in any of  $15!$  permutations, including the following sequences:

$$I1 = (v0, v8, v1, v9, v2, v10, v3, v11, v4, v12, v5, v13, v6, v14, v7, v15), \quad (6)$$

$$I2 = (v15, v1, v14, v2, v13, v3, v12, v4, v11, v5, v10, v6, v9, v7, v8, v0), \quad (7)$$

$$I3 = (v5, v8, v14, v2, v3, v11, v15, v1, v13, v0, v4, v12, v9, v6, v10, v7). \quad (8)$$

The first and second LFSR configurations, 112A and 112B, include eight rising edge (positively triggered) D-flipflops and eight falling edge (negatively triggered) D-flipflops. Alternatively, the rising edge and falling edge FF signals can be exchanged with each other.

At least three unusual features are relied upon in this invention. First, feedback from a rising edge LFSR configuration is received by a falling edge LFSR configuration, and conversely. Second, The FFs within each of the first

and second LFSR configurations operate without an input tap. Individually, the first and second LFSR configurations do not operate as standard LFSRs in Figure 2. Third, at least one of (and preferably both of) the two LFSR configurations, 112A and 112B, should correspond to an irreducible polynomial, but the system will work where only one of the two characteristic polynomials is irreducible. If each of the two characteristic polynomials is a different irreducible polynomial, the minimum cycle length becomes 65,535.

The three-input and four-input AND gates, 121 and 123, or 161 and 163, in Figure 2 can be replaced by two AND gates with  $m1$  and  $7-m1$  input terminals, respectively, where  $m1 = 2, 3, 4$  and  $5$ .

Figure 3 schematically illustrates a system 211 for generating a 16-bit PRN  $S(t;out)$  within one clock cycle according to another embodiment of the invention, using a first 8-bit LFSR 212A that is triggered on a rising clock signal edge and a second 8-bit LFSR 212B that is triggered on a falling clock signal edge during the same clock cycle. The first and second LFSR configurations shown in Figure 32 correspond to the respective irreducible characteristic polynomials

$$pA(x;8) = 1 + x^2 + x^3 + x^5 + x^8, \quad (9A)$$

$$pB(x;8) = 1 + x^2 + x^3 + x^5 + x^8. \quad (9B)$$

Signals for the LFSRs 212A and 212B preferably transition during a rising clock signal edge and during a falling clock signal edge, respectively, or during a falling clock signal edge and during a rising clock signal edge, respectively. The particular irreducible characteristic polynomials,  $pA(x;8)$  and  $pB(x;8)$ , set forth in Eqs. (9A) and (9B), implemented as shown in the LFSR configurations of Figure 3, are another example of a degree-eight characteristic polynomial. Optionally, the output signals from the FFs 217-i and/or the output signals from the FFs 257-i



( $i = 0, 1, \dots, 7$ ) are passed through delay modules with selected time delays to control any race problem that might otherwise occur.

Each of the first LFSR configuration 212A and the second LFSR configuration 212B performs as discussed in connection with the analogous LFSRs, 112A and 112B, in Figure 2, but with a different characteristic polynomial, set forth in Eqs. (9A) and (9B).

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